One Chip Telephone Circuit

Description

TELEFUNKEN microelectronic's one chip telephone circuit, U 3750 BM, is BICMOS integrated circuit that performs all the speech and line interface functions required in an electronic telephone set, the tone ringer, the pulse and DTMF dialling with redial, a keyboard interface with the possibility to interface with an external microcontroller using the internal serial bus, and a power supply for peripherals.

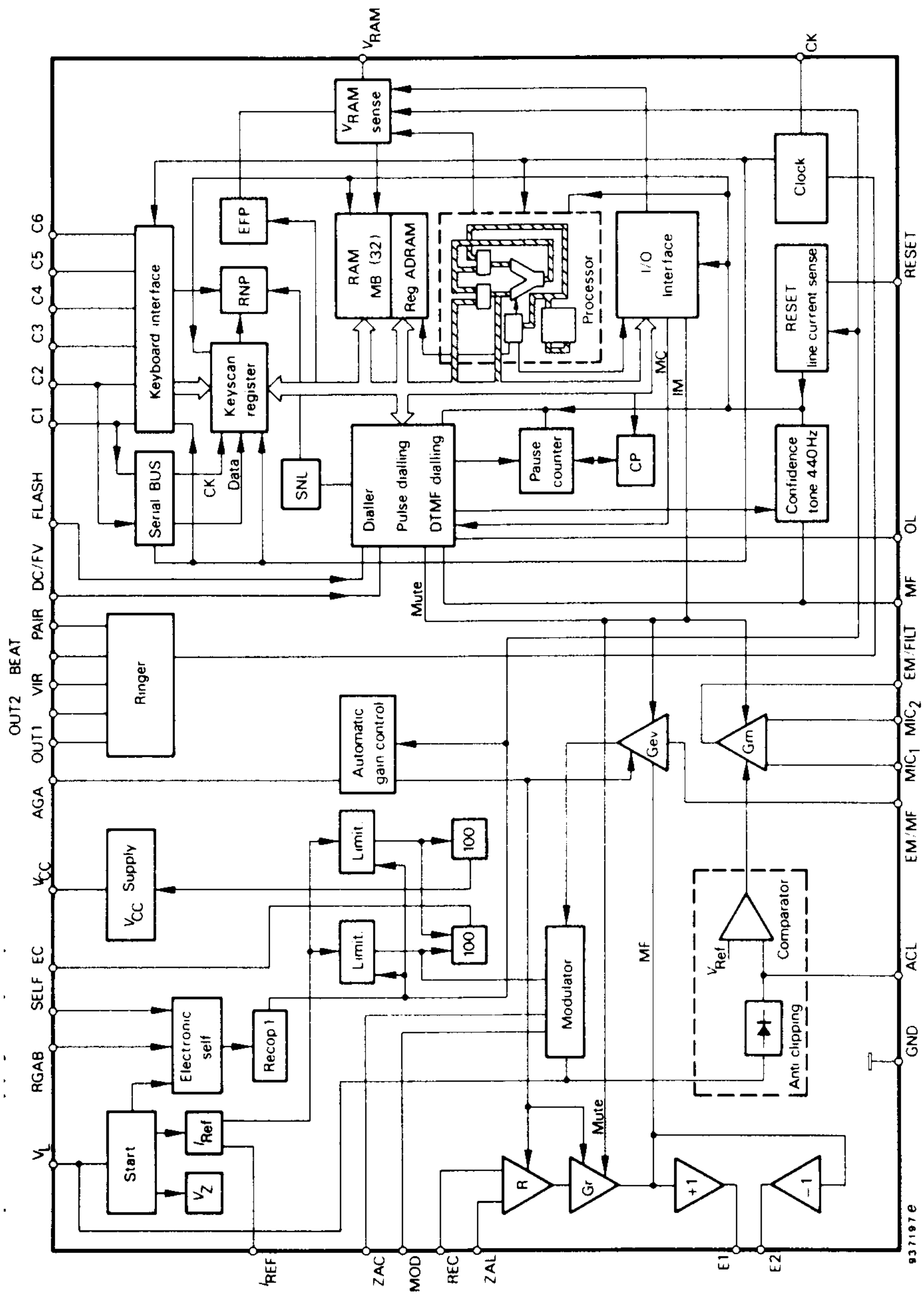
Features

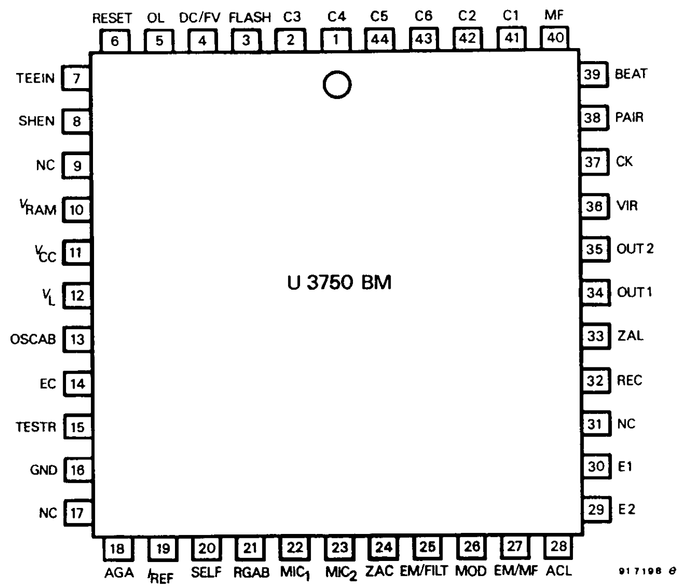
- Adjustable dc slope characteristic
- Adjustable automatic line length receiving and sending gain control (not used in DTMF) with the possibility of fixed gain (PABX)
- Adjustable dynamic impedance
- Stabilized power supply for peripherals
- Confidence level during pulse and DTMF dialling
- Receiving amplifier for dynamic or piezo-electric ear pieces
- High-impedance microphone inputs (80 kΩ in symmetrical and 40 kΩ in asymmetrical) suitable for dynamic, magnetic, piezo-electric or electret microphone
- Dynamic limiting in sending (anticlipping) prevents distortion of line signal and sidetone
- Ringing balanced output in HVMOS for higher power capability
- Four ringing tones adjustable without external components
- Internal speed up circuit permits a faster charge of V_{CC} and V_{RAM} capacitors
- Logic bounce elimination
- Pulse dialling 66/33 or 60/40 or DTMF dialling selectable by programming pin
- Adjustable flashing duration
- Pause function
- Confidence tone (440 Hz)
- Last number redial up to 23 digits
- Standard low-cost ceramic 455 kHz
- Binary data input in serial mode
- Test-mode capability.

Benefits

- Low number of external components
- High quality through one chip solution

Block Diagram



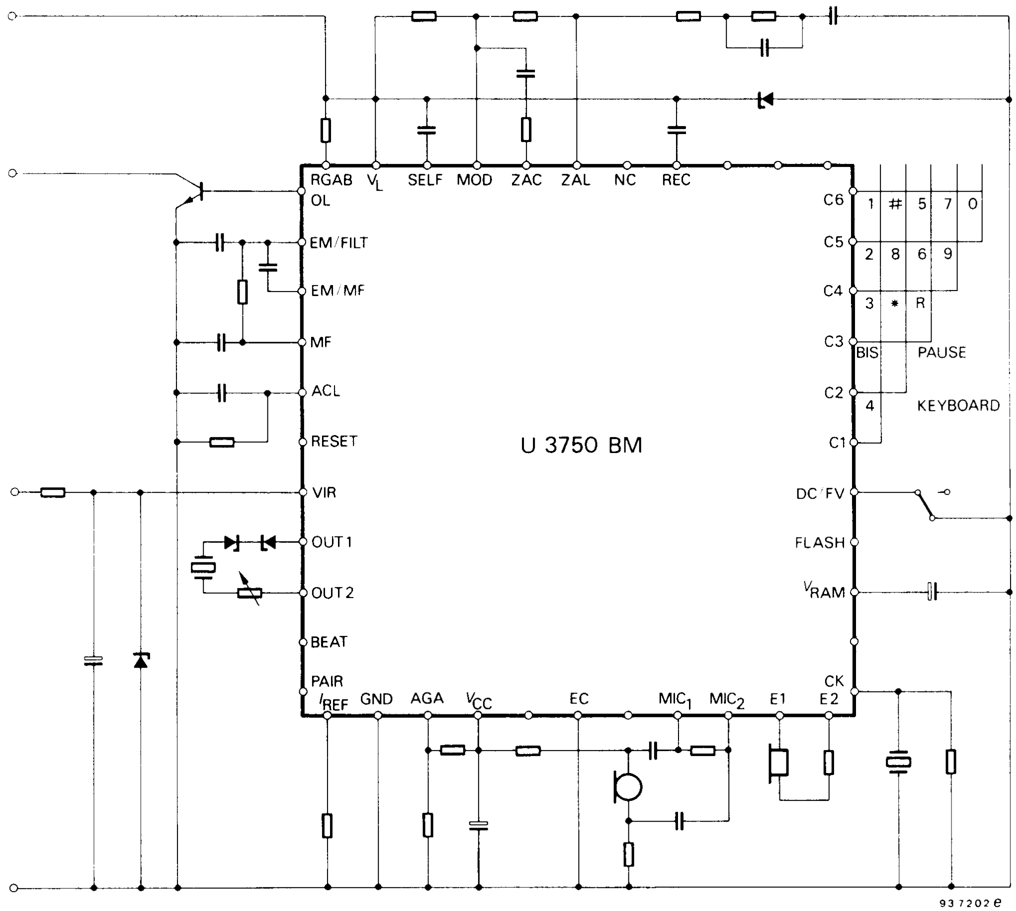


Pin Description

Pin	Symbol	Function
1	C4	Keyboard input
2	C3	Keyboard input
3	FLASH	Flashing selection
4	DC/FV	Dialling selection (33/66 pulse, 40/60 pulse or DTMF)
5	OL	Open line output
6	RESET	Output reset
7	TEEIN	Test pins
8	SHEN	Test pins
9	NC	Not connected
10	V_{RAM}	RAM and internal logic supply
11	V_{CC}	Power supply for peripherals
12	V_L	Line voltage
13	OSCAB	Test pin
14	EC	Extra current for peripherals or can be used to dissipate power for high line current applications.
15	TESTR	Test pin
16	GND	Ground
17	NC	Not connected
18	AGA	Line length AGC adjustment
19	I_{REF}	Bias adjustment
20	SELF	Electronic self input
21	RGAB	DC characteristic slope adjust-ment
22	MIC_1	Microphone input

Pin	Symbol	Function
23	MIC_2	Microphone input
24	ZAC	Dynamic impedance adjustment
25	EM/FILT	First sending stage output
26	MOD	Modulator output
27	EM/MF	Second sending stage input and DTMF input
28	ACL	Anticlipping time constant ad-justment
29	E2	Receiver output
30	E1	Receiver output
31	NC	Not connected
32	REC	Receiver input
33	ZAL	Sidetone network
34	OUT1	Buzzer output
35	OUT2	Buzzer output
36	VIR	Ringing supply
37	CK	Ceramic input (455 KHz)
38	PAIR	Adjustment between two pairs of ringing frequencies
39	BEAT	Beat adjustment of each pair of ringing frequencies
40	MF	DTMF output
41	C1	Keyboard inputs
42	C2	Keyboard inputs
43	C6	Keyboard inputs
44	C5	Keyboard inputs

Application Circuit



Absolute Maximum Ratings

See application circuit

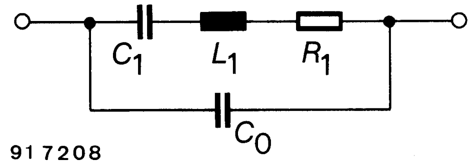
Parameters		Symbol	Value	Unit
DC line voltage	Pin 36	VIR	35	V
DC line current	Pin 36	IR	30	mA
Conversation line voltage	Pin 12	V_L	15	V
Pulse duration, t = 20 ms		V_L	17	V
Conversation line current	Pin 12	I_L	150	mA
Power dissipation, T_{amb} = 55°C		P_{tot}	1	W
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	–25 to +55	°C
Storage temperature range		T_{stg}	–55 to +155	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	70	K/W

Electrical Characteristics

f = 1 kHz, f_{clock} = 455 kHz, R_E = 20 kΩ, T_{amb} = 25°C, unless otherwise specified, Q (Resonance factor) = 3100, L_1 = 6.1 mH, C_1 = 21 pF, C_O = 268.5 pF, R_1 = 5.5 Ω. All resistances are specified at 1%, all capacitance at 2%.



Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Line voltage normal Line voltage operation	I_L = 8 mA I_L = 15 mA I_L = 28 mA I_L = 60 mA figure 3	V_L	2.9 4.1 6.4 12.3	 4.5	3.6 4.9 7.3 13.7	V
Stabilized voltage	I_L = 8 mA, I_{CC} = 0.6 mA I_L ≥ 28 mA, I_{CC} = 2.1 mA figure 3	V_{CC}	2.0 3.3	2.5 3.5	 3.7	V
Transmission						
Sending gain AGC	V_{MI} = 2 mV_{RMS} (note 1) I_L = 28 mA (G_S max) I_L = 60 mA (G_S min) I_L = 28 to 60 mA figure 3	 G_S ΔG_S	 47 39.5 –6	 48 41 –7	 49 42.5 –8	 dB
Psophometric sending noise	V_{MI} = 0, I_L = 28 mA figure 3			–73	–68	dBmp
Attenuation gain during dialing	V_{MI} = 2 mV_{RMS}, I_L = 28 mA figure 3	A_S	63			dB
Microphone input impedance (Pins 22–23)	figure 3		70	120		kΩ
Common mode rejection ratio	I_L = 28 mA figure 3	CMRR		80		dB
From transmission to dialing mode	I_L = 28 to 60 mA figure 3, Pin 25	Step	–100		+100	mV
Dynamic limiter (anticlipping) Output voltage swing (peak-to-peak value)	C_{ACL} = 470 nF, R_{ACL} = 6.8 MΩ I_L = 20 mA I_L ≥ 28 mA, V_{MI} = 8 mV_{RMS} figure 3		 3.0	 2.5 3.6	 4.2	V_{pp}
Overdrive dynamic range	I_L ≥ 28 mA figure 3				5	dB
Line distortion (on 600 Ω)	I_L ≥ 28 mA V_{MI} = 4.6 mV_{RMS} V_{MI} = 8 mV_{RMS} V_{MI} = 80 mV_{RMS} figure 3				 3 5 5	%

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Available current	Close switch S4 I_L = 28 mA I_L = 60 mA figure 3 Pin 14		7.0 35	8 40		mA
Reception						
Receiving gain $G_R = V_R/V_L$ AGC	V_L = 0.3 V_{RMS} I_L = 28 mA (G_R max) I_L = 60 mA (G_R min) I_L = 28 to 60 mA figure 4	G_R ΔG_R	10 2.5 –6	11 4 –7	12 5.5 –8	dB
Psophometric receiving noise	V_L = 0V, I_L = 28 mA figure 4 Pin 29–30				–65	dBmp
Receiving distortion	I_L = 15 mA, V_R = 2.8 V_{pp} I_L = 28 mA, V_R = 5.5 V_{pp} I_L = 60 mA, V_R = 5.0 V_{pp} figure 4				3 3 3	%
Receiver output impedance	V_R = 50 mV_{RMS}, I_L = 28 mA figure 4 Pin 29–30		45	65	85	Ω
Receiver output offset	I_L = 28 mA figure 4 Pin 29–30		–650		+650	mV
Sidestone (V_R/V_M)	I_L = 28 mA figure 3			36	40	dB
Z line matching impedance	V_L = 0.3 V_{RMS} I_L = 28 and 60 mA figure 4		580	660	750	Ω
Ringer						
Turn on voltage	Measured at pin VIR figure 5	V_{ON}		16	18.0	V
Turn off voltage	figure 5	V_{OFF}	9.5	10.5		V
Current consumption without load	VIR = 18 V			1.2	1.5	mA
Output voltage swing	Load = 10 kΩ figure 5	V_{OUT}	VIR–2			Vp
Output tone frequencies	Pin 38 grounded Pin 38 open			1458 1166 547 438		Hz
Sweep frequencies	Pin 39 grounded Pin 39 open			4.0 9.1		Hz
Leakage current	VIR = 30 V II_L at VI_L = 0 V Pins 38 and 39 figure 5				5	μA

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DTMF generation Pin 4 grounded						
Tone frequency accuracy (confidence tone included)	V_{RAM} = 3.5 V		–0.4		+0.25	%
Low group tone level (depends on external components)	(Note 2) Measured on 600 Ω I_L = 28 mA figure 3		–10	–8	–6	dBm
High group tone level (depends on external components)	(Note 2) Measured on 600 Ω I_L = 28 mA figure 3		–8	–6	–4	dBm
Preemphasis (depends on external components)	(Note 2) Measured on 600 Ω I_L = 28 mA figure 3		1	2	3	dB
DTMF distortion (depends on external components)	(Note 2 and note 3) Measured on 600 Ω I_L = 28 mA, 300 < f < 3400 Hz figure 3				3.5	%
DTMF transmission time DTMF interdigit time		t_{MF} t_{IMF}	80.2 89.2		82.4 89.2	ms ms
Transmission mute tm_{MF}			169.4		171.6	ms
Confidence tone	Only by serial bus					
FCT frequency				440.9		Hz
Tone level (depends on external components)	Measured on 600 Ω I_L = 25 mA figure 3			–9		dBm

Note 1: sending gain: $G_S = V_L/V_{MI}$ with the values of R_{AG1} and R_{AG2} (figure 3) so the maximum gain is at 28 mA and the minimum gain is at 60 mA.

Note 2: For DTMF measurements, close switches S1 and S3 and select each group of frequencies on the keyboard.

Note 3: The level of each harmonic on line is under the limited curve given below with the filter components value chosen for the test.

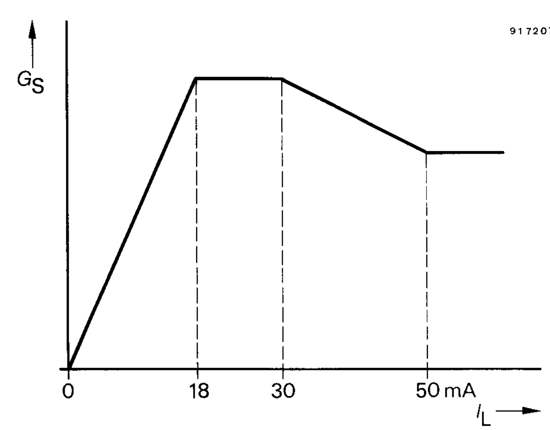


Figure 1

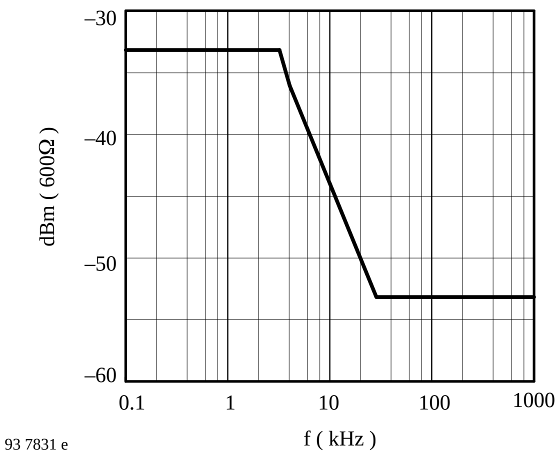


Figure 2 DTMF Distortion

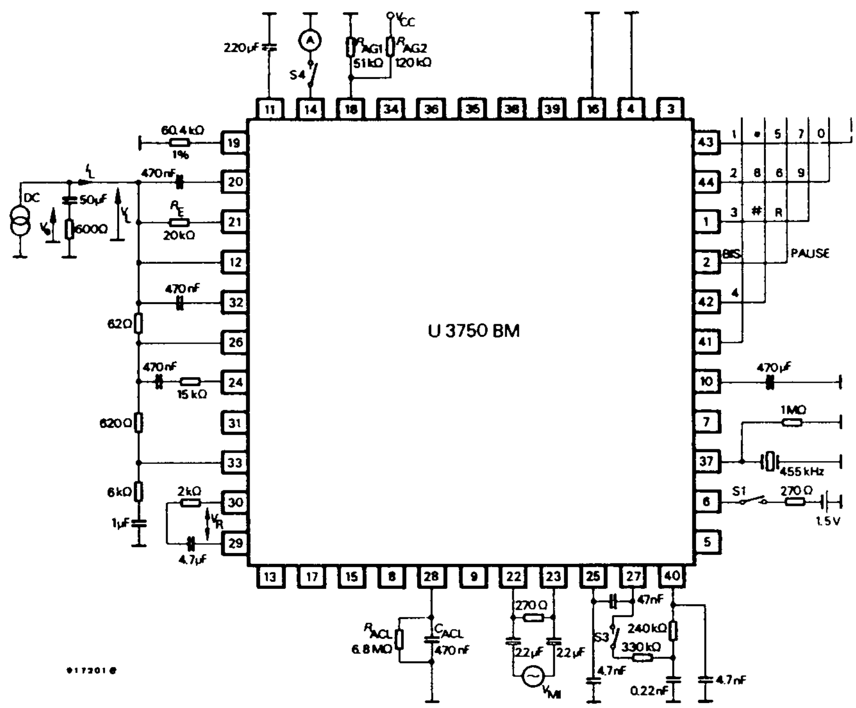


Figure 3 Test Circuit

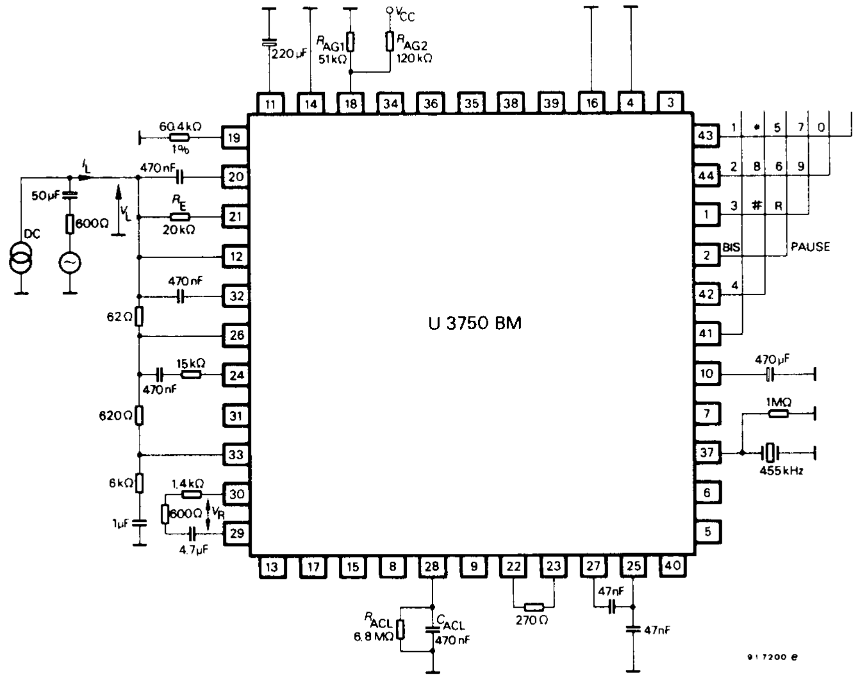


Figure 4   Test circuit

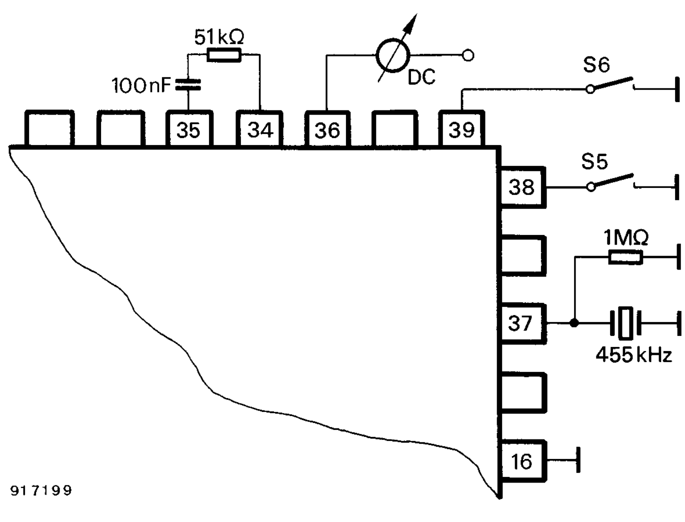


Figure 5   Test circuit

S_5 (Pin 38)	S_6 (Pin 39)	Pair of frequencies (Hz)	Sweep frequency (Hz)
ON	ON	1458/1166	4
ON	OFF	1458/1166	9.1
OFF	ON	547/438	4
OFF	OFF	547/438	9.1

Electrical Characteristics of Logical Part

f_{clock} = 455 kHz (other specifications as under electrical characteristics).

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
V_{RAM}			2.4	2.75	2.9	V
Speed-up off threshold	I_L = 8 mA	V_{SOFF}	1.9	2.2	2.3	V
Speed-up on threshold	I_L = 15 to 70 mA	V_{SON}		2.5		V
Logic operating voltage in normal mode				3.5		V
I_{RAM}						
Oscillator on	V_{RAM} = 3.5 V				800	µA
Leakage					300	µA
Inputs: C1, C2, C3, C4, C5, C6, DC/FV, FLASH	Input voltage low, V_{IL}				0.2	V
	Input voltage high, V_{IH}		0.8 V_{RAM}		V_{RAM}	V
Keyboard pins: C1, C2, C3, C4, C5, C6						
Internal pull down	V_{IL} = 3.5 V		15		50	µA
Output current	V_{IH} = 0 V		0.8		2.5	µA
FLASH, DC/FV						
Internal pull-up current IPV	V_{IL} = 0 V		0.5		5	µA
Leakage current	V_{IH} = 3.5 V				1	µA
Timing and frequency						
Reset time t_r (see figure 6 and 7)	In mode 60/40			30		ms
	In mode 66/33 and DTMF mode			33		ms
Clock start-up time t_{on}				5		ms
Time line break generating a reset: t_{lb}	In mode 60/40		290		300	ms
	In mode 66/33 and DTMF mode		319		330	ms
Debounce time, t_e	In mode 60/40		14	24	34	ms
	In mode 66/33 and DTMF mode		15.4	26.4	37.4	ms
RESET output (with 390 Ω series)						
Output low current	V_{OL} = 2.5 V	I_{OL}	0.25		1.2	mA
Output high current	V_{OL} = 0.5 V	I_{OH}	0.25		1.2	mA
OL output						
Output low current	V_{OL} = 0.5 V	I_{OL}	2		20	µA
Output high current		I_{OH}	1		4	mA
MF output						
High impedance	V_{OHI} = 1.4 V				0.5	µA
	FL = L, FH = H, V_{OH} = 3.5 V		150		350	µA
	FB = L, FH = H, V_{OH} = 0 V		200		550	µA
	FB = H, FH = L, V_{OH} = 3.5 V		200		550	µA
	FB = H, FH = L, V_{OH} = 0 V		150		350	µA
CK Input						
Low input leakage	V_{IL} = 0.5 V				1	µA
High input leakage	V_{IL} = 3.0 V				1	µA

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Serial bus (see figure 12)						
Pulse width clock		t_{wl}, t_{wh}	2			µs
Pulse width enable signal		t_{el}, t_{eh}	2			µs
Set-up time data to clock		$t_{set\ up}$	0			µs
Hold time data from clock			100			µs
Enable time		t_e	0			µs
Time between two transmissions		t_{RRN}	900			µs
Pulse dialing (OL) Dialing pulse frequency	In mode 60/40 (Pin 4 tied to RESET)			10		Hz
	In mode 66/33 (Pin 4 not connected)			10.11		Hz
Dialing pulse period		T_{OL}		100		ms
				98.9		ms
Break time		t_b		60		ms
				66		ms
Make time		t_m		40		ms
				33		ms
Interdigit time		t_{IDOL}	830		833	ms
			813		816.5	ms
Transmission mute: $t_{mol} = (t_m + t_b) \cdot n + t_{m1}$			[n · 100 + 30]		(n · 100)+ 32	ms
n pulses dialling			[n · 98.8 + 22]		(n · 98.9) + 24.2	ms
Flash pulse						
Flash pulse duration	Pin 3 to GND Pin 4 to RESET	t_{fl}	89.5		92	ms
	Pin 3 to GND Pin 4 to NC		98.5		101	
	Pin 3 to GND Pin 4 to GND		102.5		105	
	Pin 3 to NC Pin 4 to RESET		239.5		242	
	Pin 3 to NC Pin 4 to NC		263.5		266	
	Pin 3 to NC Pin 4 to GND		274.0		277	
	Pin 3 to RESET Pin 4 to RESET		109.5		112	
	Pin 3 to RESET Pin 4 to NC		120.5		123	
	Pin 3 to RESET Pin 4 to GND		125.0		128	
Transmission mute	In mode 60/40	tm_{fl}	830		832	
	In mode 66/33		813		815.5	
	In mode DTMF		846		848.5	
Pause time	In mode 60/40	T_p	3116		3118	ms
	In mode 66/33		3075		3077	ms
	In DTMF mode		3012		3110	ms

Power-on Reset and Pin RESET

To avoid undefined states of the device when it is powered on, an internal reset clears the control logic. When the power supply rises above the internal reference level, the pin RESET goes to high during t_{rt}. After a line break longer than t_{lb}, a reset is generated. A short line break (< t_{lb}) does not affect the reset. Power on reset timings (t > t_{lb}).

1) $V_{RAM} > V_{SON}$ at t = 0 . . . . a)

Trt = Tr + T on . . . . b)

a)

b)

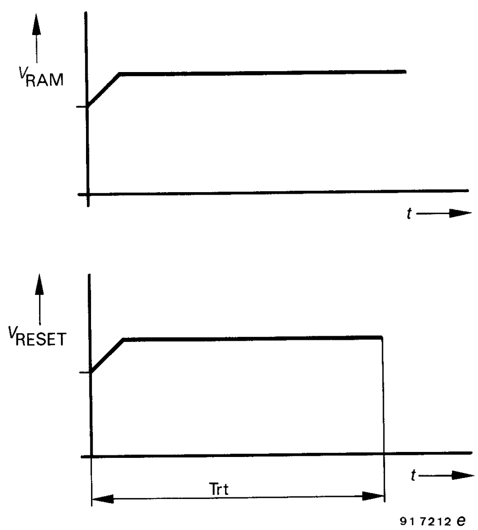


Figure 6

2) $V_{RAM} < V_{SON}$ at t = 0 . . . . a)

Trt = T (V_{RAM} to $V_{S\ off}$) + Tr + T on . . . . b)

a)

b)

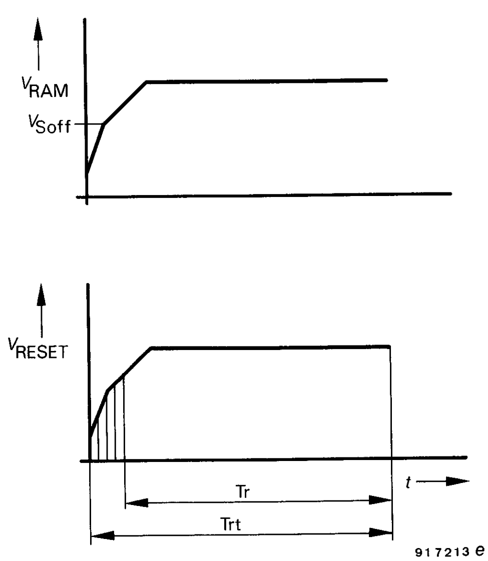


Figure 7

Pin RESET

It is the power on reset output.

In test mode, it permits to force the IC U 3750 BM in permanent DTMF dialing by applying a negative voltage (test schematic figure 3).

Data Acquisition

Input data is derived from any standard matrix keyboard (15 keys) or from a remote microcontroller.

Keyboard

The keyboard is connected to the IC by six pins, (see figure 8). Its matrix is triangular.

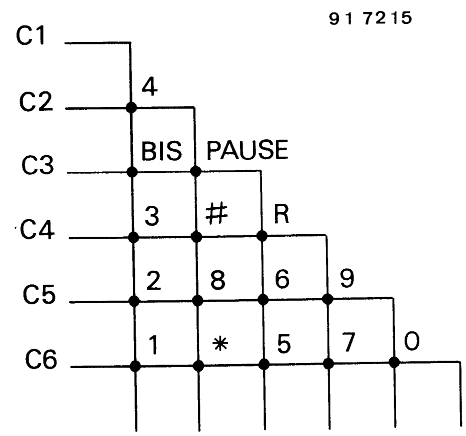


Figure 8 Keyboard inputs to the U 3750 BM

Internal pull down resistors (typical value: 120 KΩ) are connected to the inputs Ci.

A push button is made by a short-circuit of two pins among the six.

Entries are scanned every 12 ms or 13.2 ms and go to the logical state 1 during this scanning.

The scanning is inhibited as soon as a calibrated line-break is produced at the OL output.

The scanning-cycle has eight phases: six of them are reserved for the scanning of the six pins, the two others are kept for the reset of the logic keyboard (T0) and the acquisition (T7).

A push button is valid, if it is unique and if it’s pressed long enough (see table of pressed and released push buttons).

Every acquisition time, T7, the input code is decoded into 5 bits (with or without a pressed push button). The microprocessor can read it as soon as the logic keyboard has set a flag, tested about every 800 ms and which indicates that a pushbutton has been correctly detected.

Table 1 The scanning principle

Keyboard clock	2 ms	2.2 ms
Ti except T0, T1, T7	2 ms	2.2 ms
T1	1.956 ms	2.156 ms
T0 or T7	22 ms	22 ms
Scanning cycle	12 ms	13.2 ms

T0: reset of the logic keyboard

T7: acquisition of the code present at the keyboard

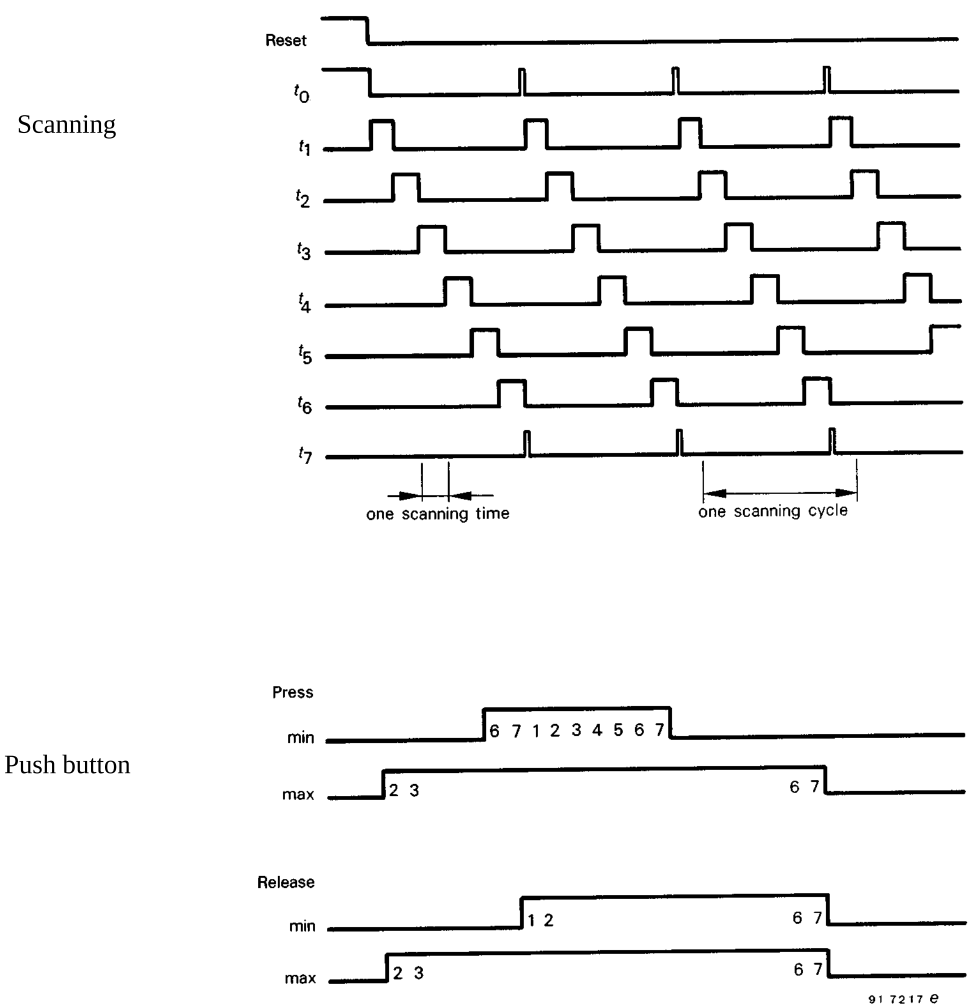


Figure 9 The scanning principle

Timing of a Push Button

The information from a pressed push button or released push button is taken into account if it is still present during at least two sampling times, T7.

Table 2 Timing of a push button

Clock keyboard 2 ms, 2.2 ms	min	typ	max	unit
Minimum time – push button on	14 15.4	24 26.4	34 37.4	ms ms
Minimum time – push button off	24 26.4	24 26.4	34 37.4	ms ms

The entries are debounced on both the leading and trailing edges for 34 ms or 37.4 ms according to the value of the keyboard clock, and so the time remains less than 40 ms. At this time the information can be processed. If the information is still present after more than 40 ms, it is only taken one time.

Serial Bus

The remote microcontroller is connected to the IC by 4 pins: C2, C3, C4, C5 (see figure 10).

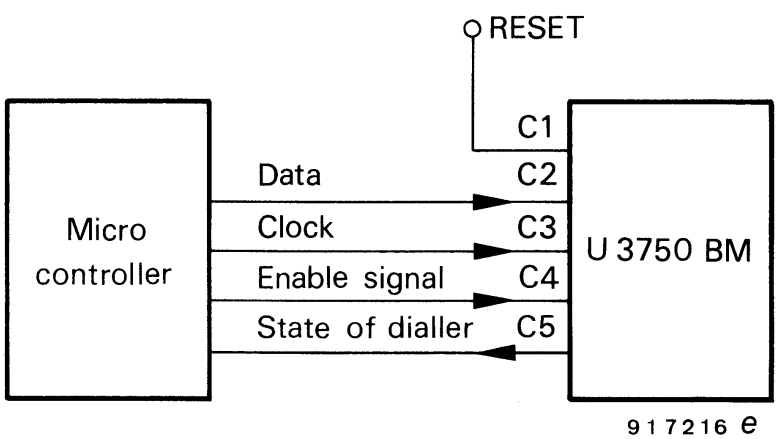


Figure 10 Connection of the microcontroller to the U3750BM

C2 transmits the data, C3 the clock, C4 the enable signal, and C5 indicates the state of the dialer:

C5 = 0, dialer is busy
C5 = 1, dialer is free

Data is serially shifted in a 5-bit register during the positive going transition of the clock pulse. The positive going transition of the enable signal validates the transmission.

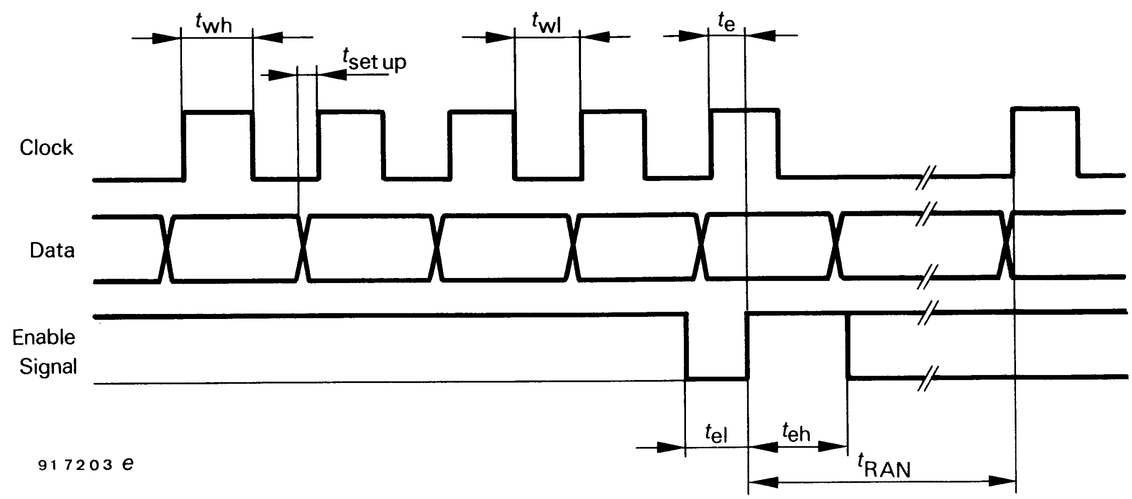


Figure 11 Timing of the serial bus

Code Entries Table

0	0	0	0	0	*
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	0
0	1	0	1	1	A
0	1	1	0	0	B
0	1	1	0	1	C
0	1	1	1	0	D
0	1	1	1	1	#
1	0	0	0	0	16
1	0	0	0	1	R flash
1	0	0	1	0	Redial
1	0	1	0	0	Confidence tone
1	0	1	0	1	Micro inhibition
1	0	1	1	0	Pause
1	0	1	1	1	23

Dialer

The IC includes a dialing circuit for either pulse dialing or dual tone multifrequency dialing. The dialer transmits the codes decoded by the logic keyboard on the outputs OL and MF.

Mode Selection

The choice of dialing is made by the tri-state-level on the DC/FV Pin

FV DC = Z	pulse dialing in 66/33 ms
FV DC tied to pin RESET	pulse dialing in 60/40 ms
FV DC = 0	DTMF dialing calibrated

When the circuit is in pulse mode, it is possible to change over to DTMF dialing with the “*” key. The code “*” is sent in line. The circuit returns in pulse mode after a reset condition or after a flash pulse (see figure 14).

Dialing Codes

The dialing codes are the numeric keys 0 to 9, and the non numeric keys A, B, C, D, *, #. All are stored in RAM. The codes A, B, C and D can be only transmitted by the serial bus. In pulse dialing, the code #, B, C and D have no effect on the dialing. The code A is filtered and corresponds to eleven pulses.

Dialing

As soon as the code is detected by the logic keyboard and written in RAM, it can only be loaded in the dialer if the dialer is not occupied and a pause is not generated.

Pulse Dialing

The output which provides control signals for proper timing in pulse dialing is pin, OL. The dialling starts with a make time (see figure 12).

Dual tone Multifrequency Dialing

The output pin, MF, provides the multifrequency signal to transmit in line. This signal results from the sum of two frequency pulses modulated and requires a filter to compose a dual sine wave. The frequencies are chosen in a low group and a high group. Table 3 shows the frequency tolerance of the output tones for DTMF signalling. In manual dialing or in redial, output tone is timed with a fixed duration.

Table 3 Frequency tolerance of the output tones for DTMF signaling

Standard Frequency	Tone Output Frequency	Frequency Deviation	
Hz	Hz	%	Hz
Low Group			
697	697.8	+0.12	+0.85
770	768.6	–0.18	–1.42
852	848.9	–0.37	–3.12
941	940.1	–0.10	–0.92
High Group			
1209	1210.1	+0.09	+1.11
1336	1338.2	+0.17	+2.23
1477	1477.3	+0.02	+0.27
1633	1636.7	+0.22	+3.69

Tone output frequency when using a 455 kHz ceramic.

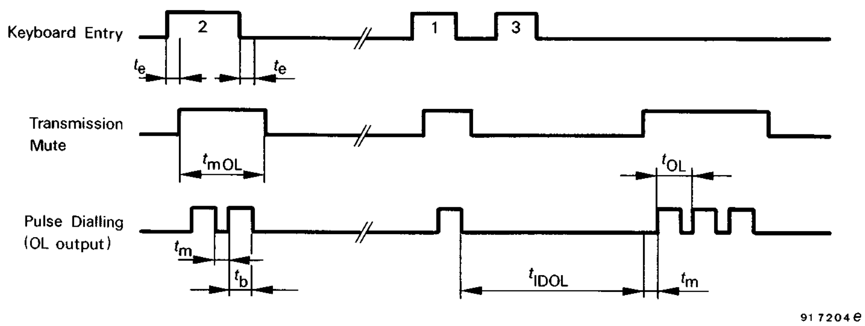


Figure 12 Timing diagram for pulse dialing

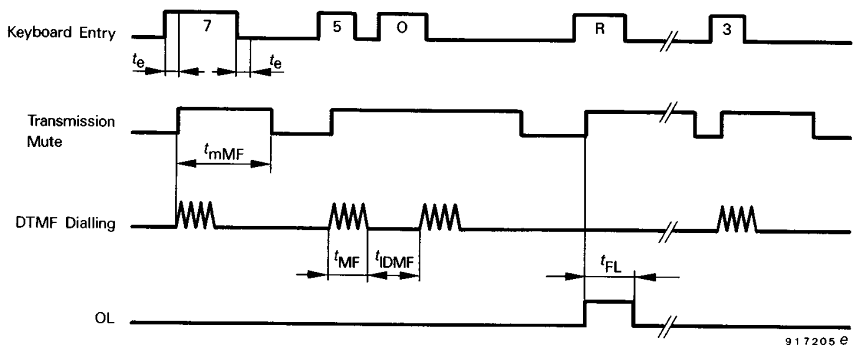


Figure 13 Timing diagram for DTMF dialing

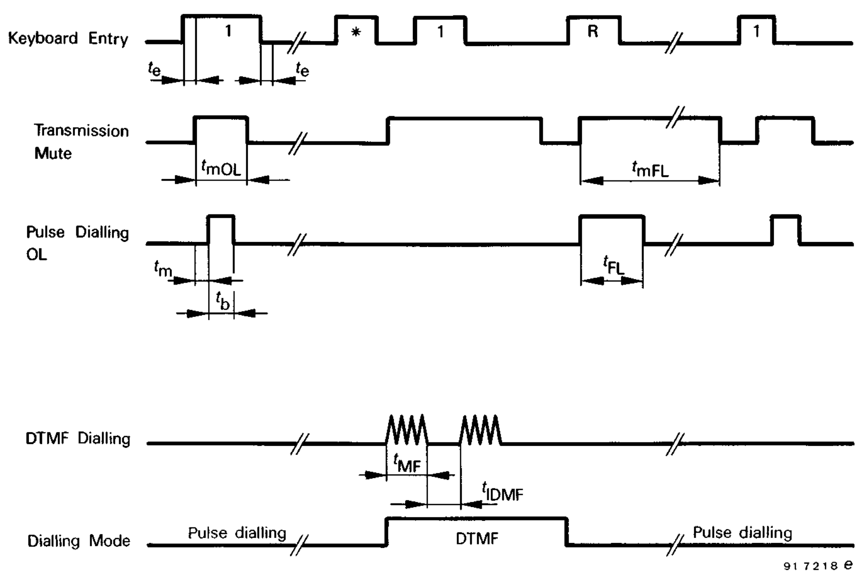


Figure 14 Timing diagram for mixed mode dialing

Flash Control

Detecting a “R” code produces either a short timed line break (< 200 ms) or long timed line break (>200 ms) at the OL output.

For the duration of the flash, it is not possible to take information from the keyboard.

Flash signifies that the circuit executes a particular work as a dialing, a redial, or a pause function, and the code “R” is lost and not used.

The flash pulse resets the read address counter and does not erase the data storage, so later redial is possible.

The flash duration is programmed by the FLASH pin (Pin 3) and depends on the selection of the tri-state-level pin (Pin 4).

Mutes (transmission mute and dialing mute) become active high from the beginning of the line break. Timings explains this.

According to these timings and what has previously been said, a second pulse flash could only follow the first one 810 ms or 850 ms later.

Consequently the “R” entry remains inhibited during a time less than 1 second.

Pause Function

A pause separates the dial sequence. It is used for waiting for a dial tone.

A pause code takes one position in the RAM like a digit. However, if the circuit executes a pause and if another pause code is entered, the storage of the second one does not occur. Furthermore, the pause running is aborted.

Duration of the pause is given in electrical characteristics for the following configuration: digit, pause, digit, and consequently takes into account the interdigit.

Particular Functions

After the reset, the particular functions are cleared. The state of the circuit is no confidence tone, no microphone inhibition.

Confidence Tone Output

When the data entries are derived from the serial bus, a pulse frequency modulation corresponding to a 440 Hz sine wave can be generated on the output MF by transmitting the confidence tone code which is 20 (in decimal). The function confidence tone is a flip-flop function.

Microphone Inhibition

Like the confidence tone, it is a flip flop function activated through the serial bus by the code 21 (in decimal).

RAM

Organization

The RAM is 32 words of 5 bits and is organized in two parts: one for the data storage and the other for the working RAM.

Safeguard

The safeguard is guaranteed by an external capacitor. If V_{RAM} decreases under the data retention supply voltage, the redial function is forbidden. After the reset of the circuit, a test is executed on V_{RAM} in order to ensure the redial validity.

Data storage

Storage, overflow and erasing are realized through three address counters. The written address counter (P1) points out the location where the code will be stored. At each storage, P1 is incremented by one. As each code is recalled from the RAM for line dialing, the read address counter (M1) is incremented by one to select the RAM location of the next code to be recalled.

Consequently, the difference between the contents of P1 and of M1 represents the number of codes that have been written into the RAM but not yet converted into line dialing.

The third counter (P2) gives the real capacity of the redial register.

Redial features

Capacity

If more than 23 codes are entered into the RAM memory, overflow results and the excess codes replace the data in the lower numbered RAM locations. In this event, automatic redial is no longer possible.

Storage

Storage pertains to the dialing codes 0 to 9, *, #, pause, A, B, C and D. It is independent of the dialing mode (pulse dialing or DTMF dialing).The storage generally contains the last digits transmitted.

Use of redial

The use of redial is always possible except if the content of the RAM is empty (P2 = 0). This happens when the RAM supply is not high enough , when an overflow occurred, or when previously an erroneous use of the redial occurred (start of manual dialing not equal to the content of the RAM).

If the redial is ordered after a manual dialing the redial is executed according to the digits already transmitted in line.

The redial is effective if the comparison digit-by-digit of all digits is correct. It is not produced if the comparison is incorrect or if the number of digits exceeded the last capacity of the redial. During redial, entry codes are accepted.

Procedure with *

Storage does not pertain to the "*" code and the codes entered after it when the manual dialing starts with a numeric code or A, B, C, D, #, or pause codes. If the dialing starts with the "*" code, all codes can be stored.

Note: the "#" code is treated for storage like a number.

Procedure with flash

The flash pulse does not reset the content of the RAM.

Example: 1 2 3 R   Redial ↕ ⇒ 1 2 3 R 1 2 3
Redial ↕ ⇒ 1 2 3

Erasing redial

The erasing is possible through the serial bus with the decimal codes 16 and 23. There is not much difference between these two codes: code 16 always erases the redial, code 23 inhibits a later redial if it is transmitted after or before dialing codes. The following examples illustrates this.

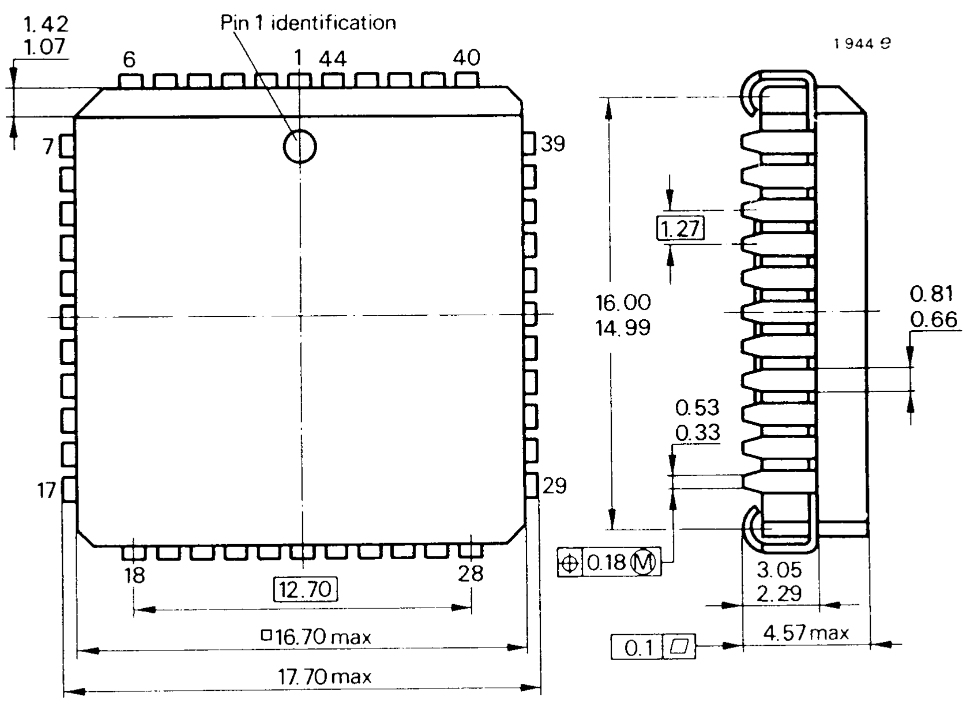
Transmitted Codes	On Line
1 2 3 (16) Redial ↕	1 2 3 –nothing
1 2 3 (23) Redial ↕	1 2 3 –
1 2 3 (16) 4 ↕ Redial ↕	1 2 3 4 4
1 2 3 (23) 4 ↕ Redial ↕	1 2 3 4 –
1 2 3 R (16)↕ Redial ↕	1 2 3 R –
1 2 3 R (23)↕ Redial ↕	1 2 3 R 1 2 3

Special Case

When the overflow flag is set and when the written address counter becomes equal to the read address counter, the codes are not stored.

Dimensions in mm

Package: PLCC 44



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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